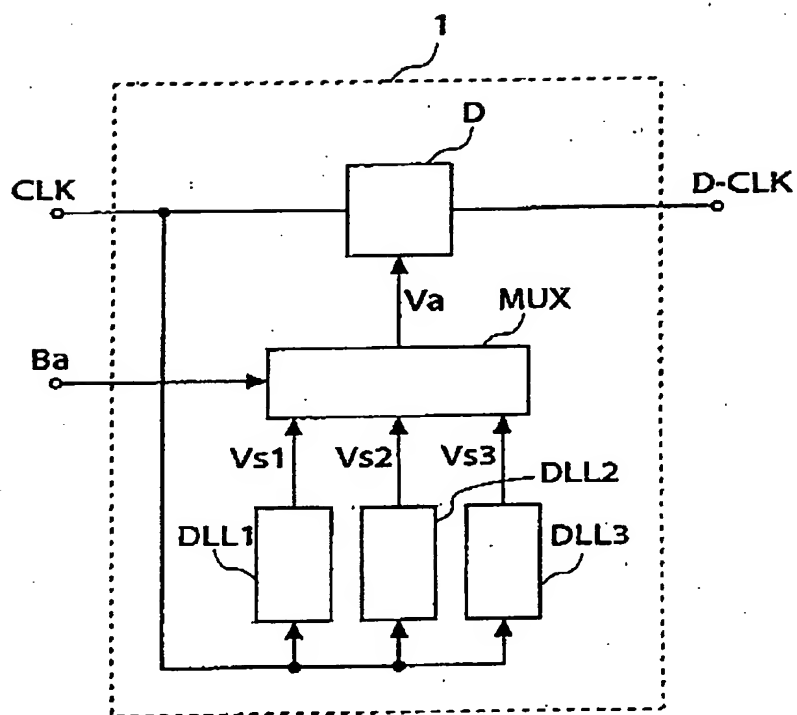


FIG. 1



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FIG. 2

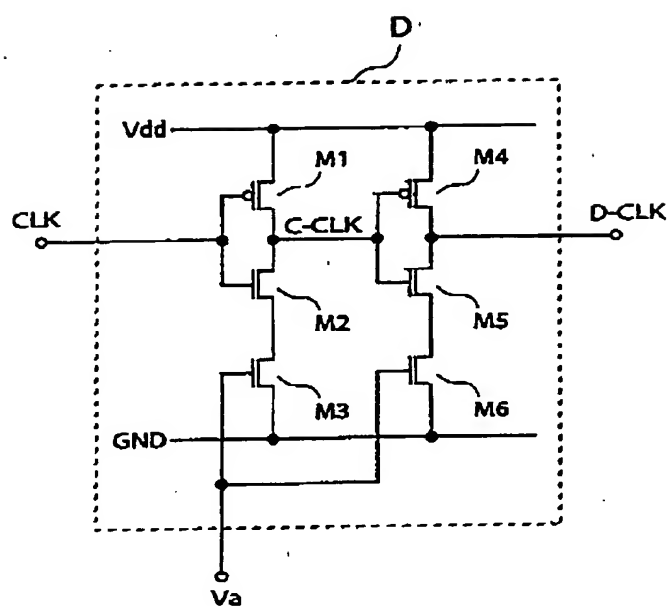
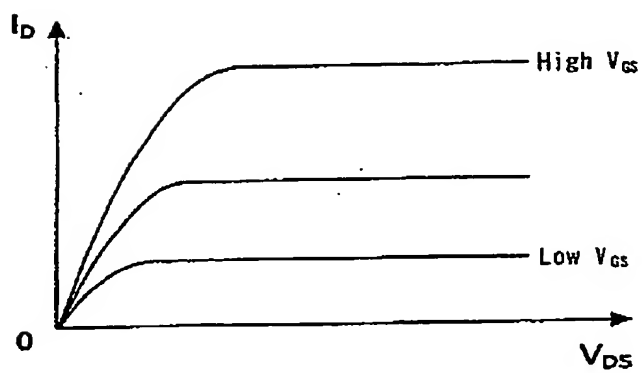


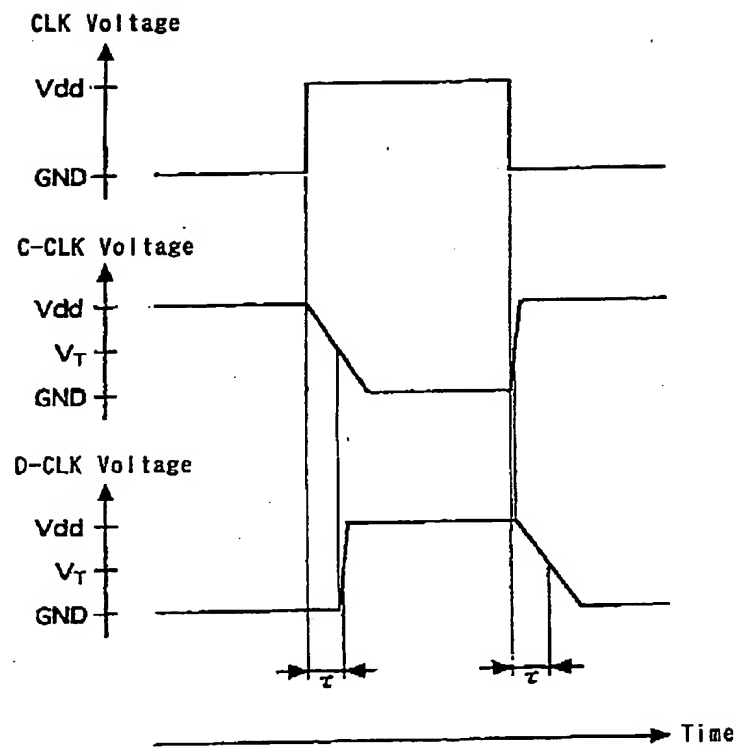
FIG. 3





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FIG. 5



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FIG. 6

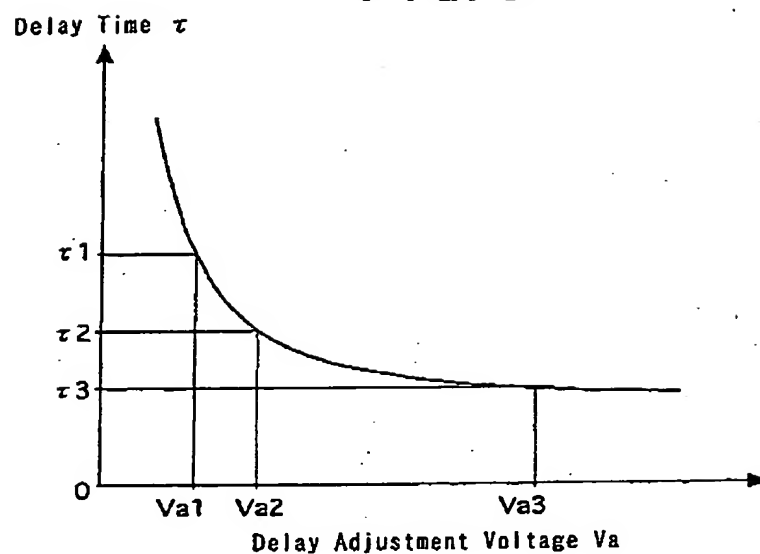
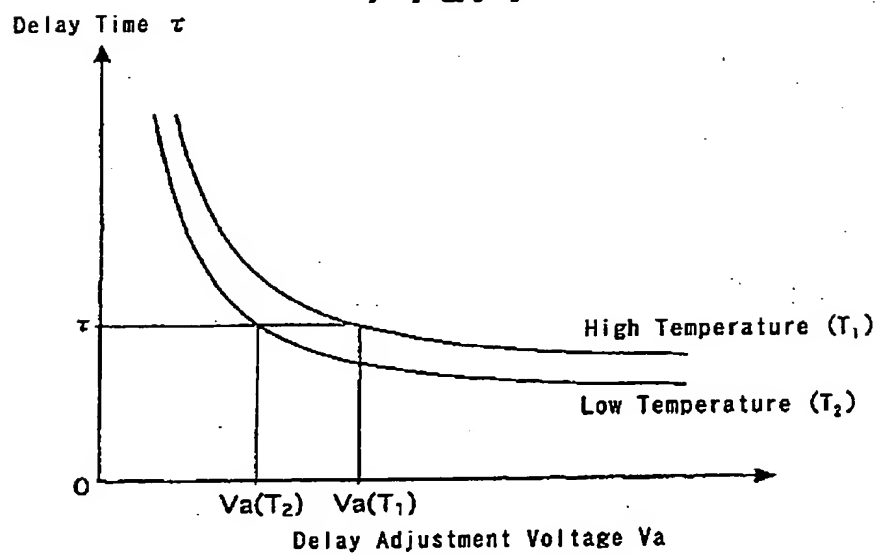


FIG. 7



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FIG. 8

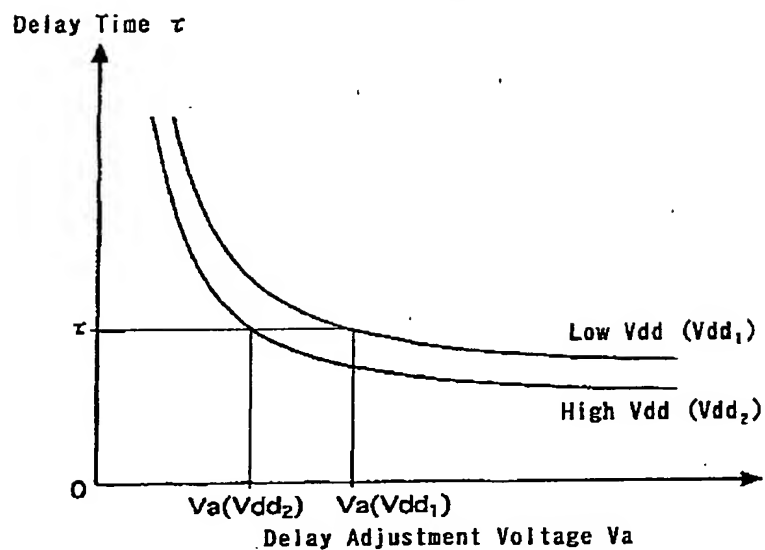
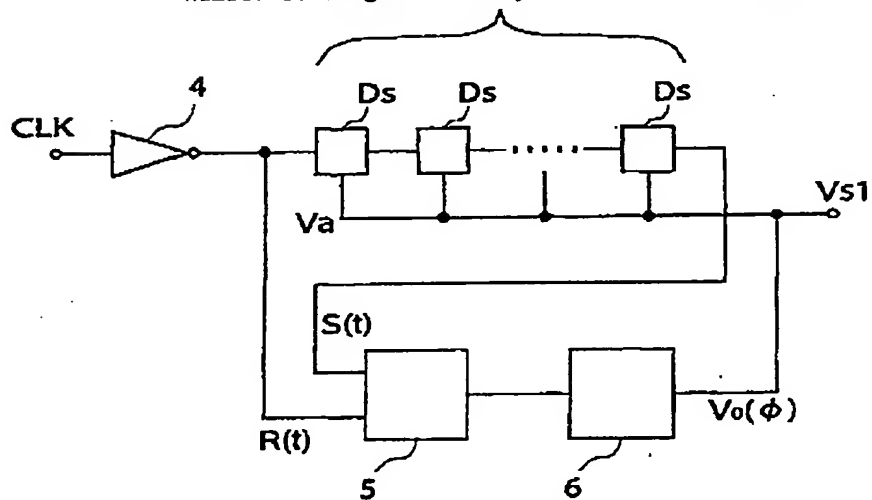


FIG. 9

Number of Stages of Delay Circuits : N1 Stages



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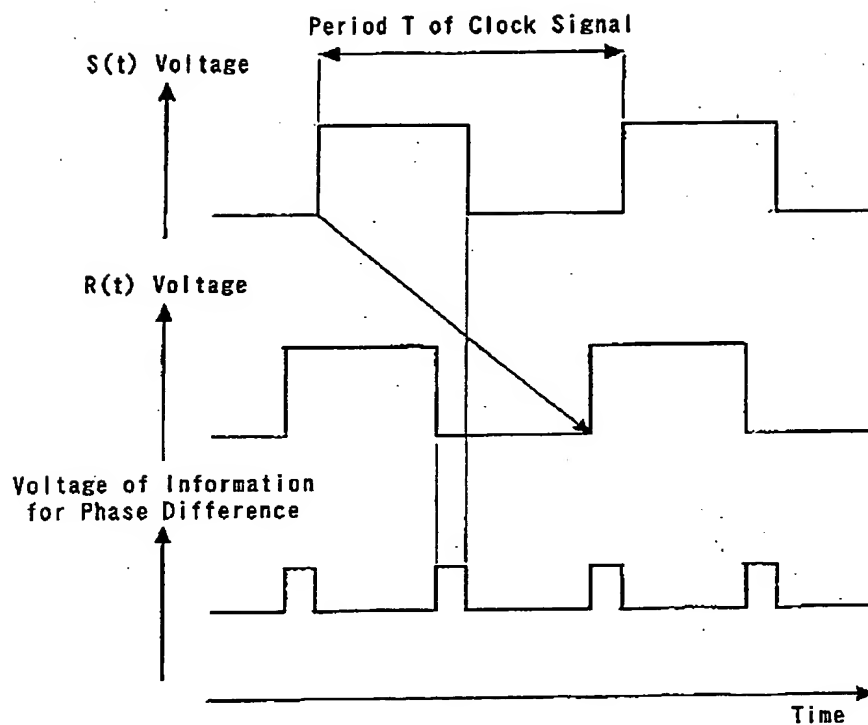
**FIG. 10**

FIG. 11

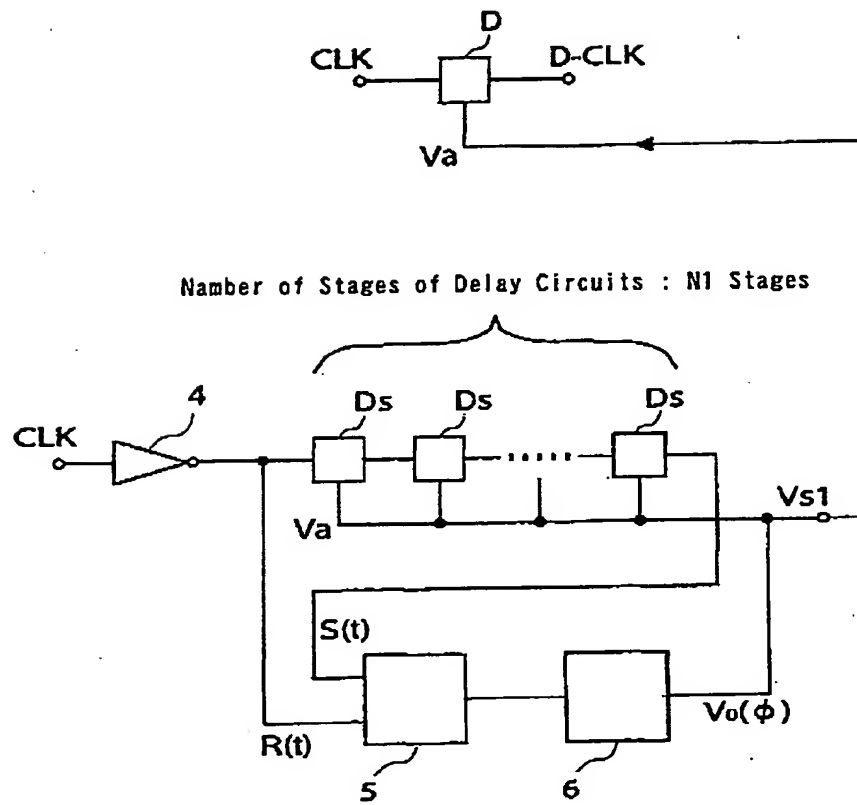
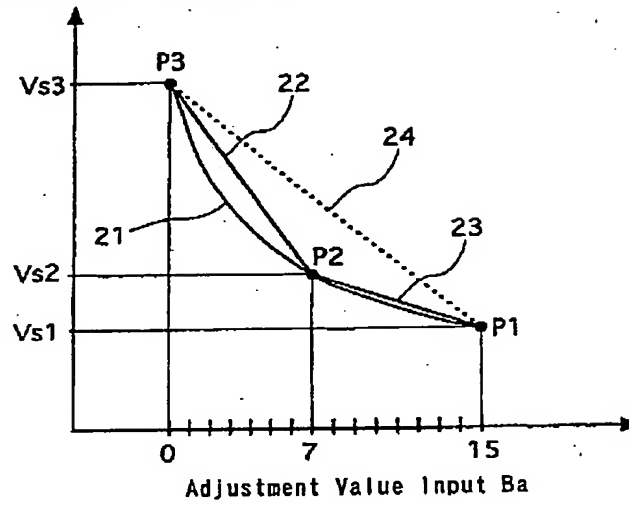




FIG. 12

Reference Adjustment Voltage  $V_s$ 

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FIG. 13

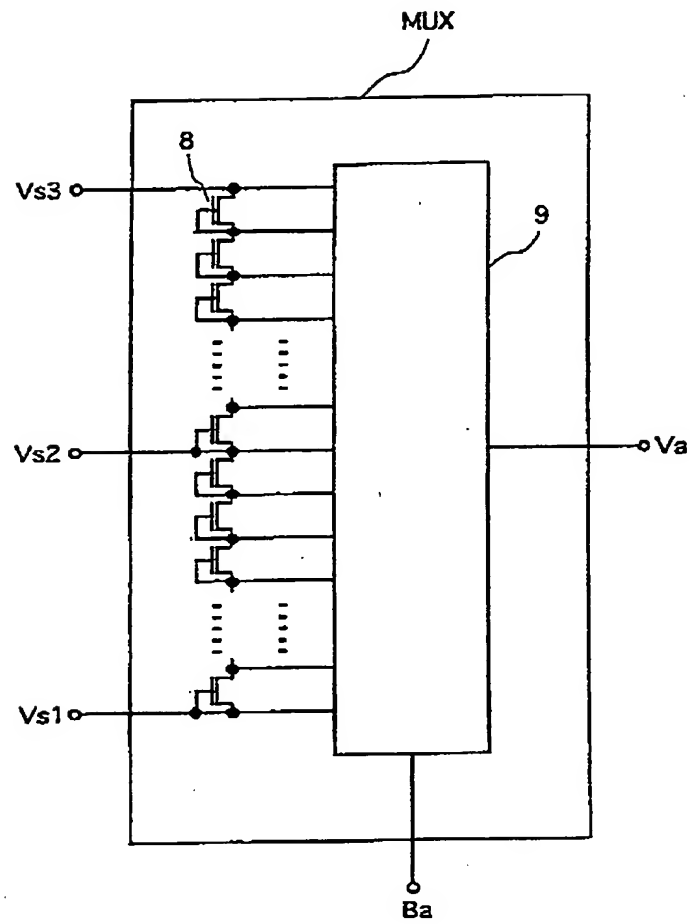


FIG. 14

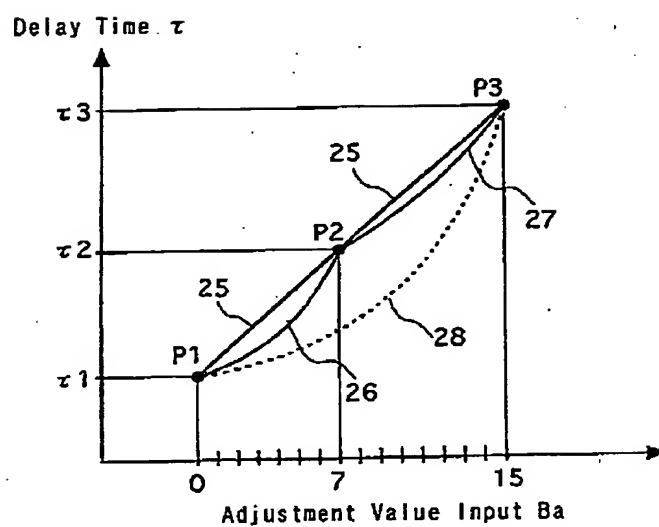


FIG. 15

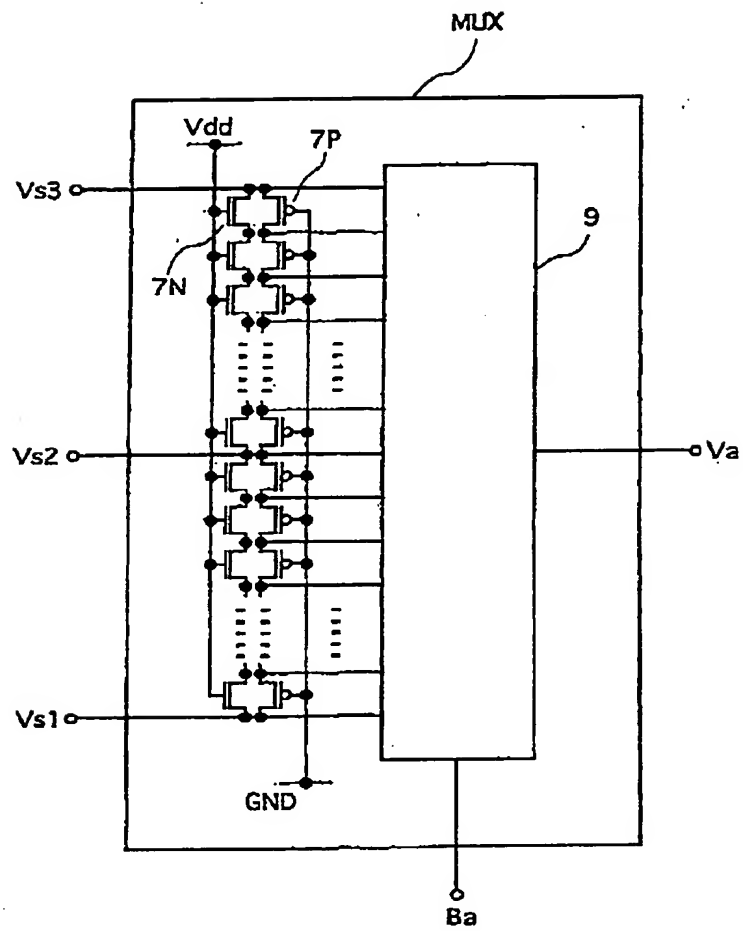


FIG. 16

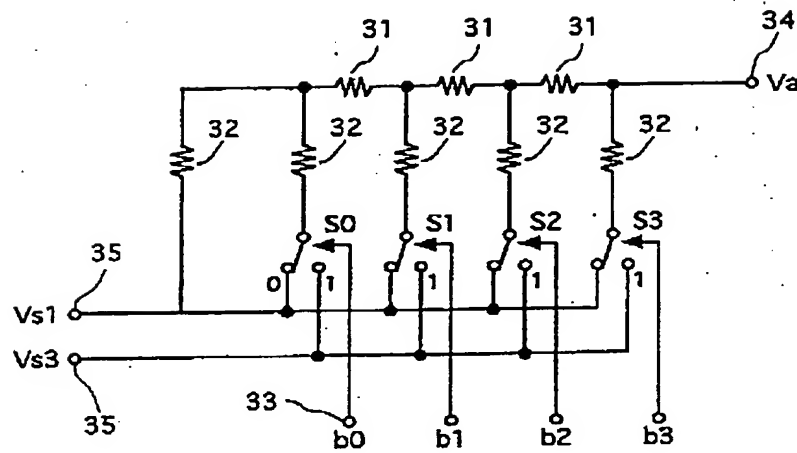
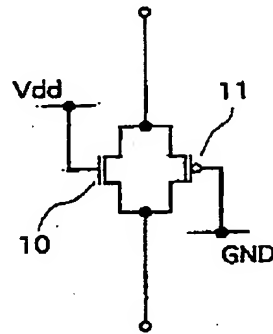


FIG. 17



**FIG. 18**

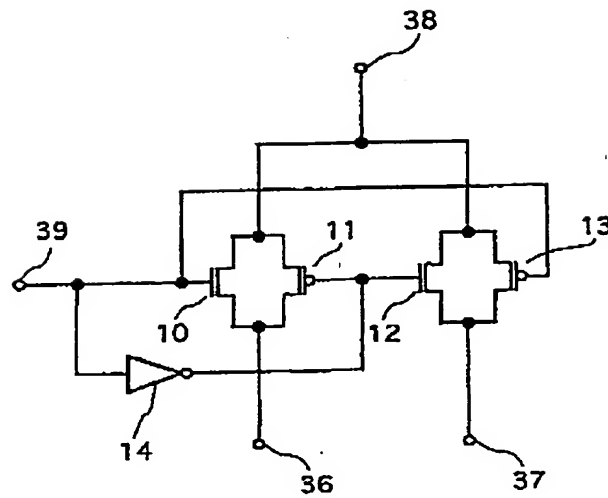
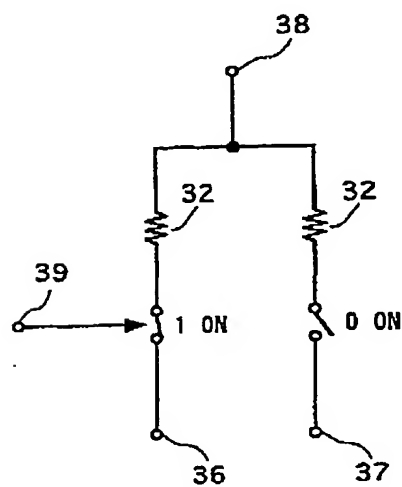


FIG. 19





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FIG. 22

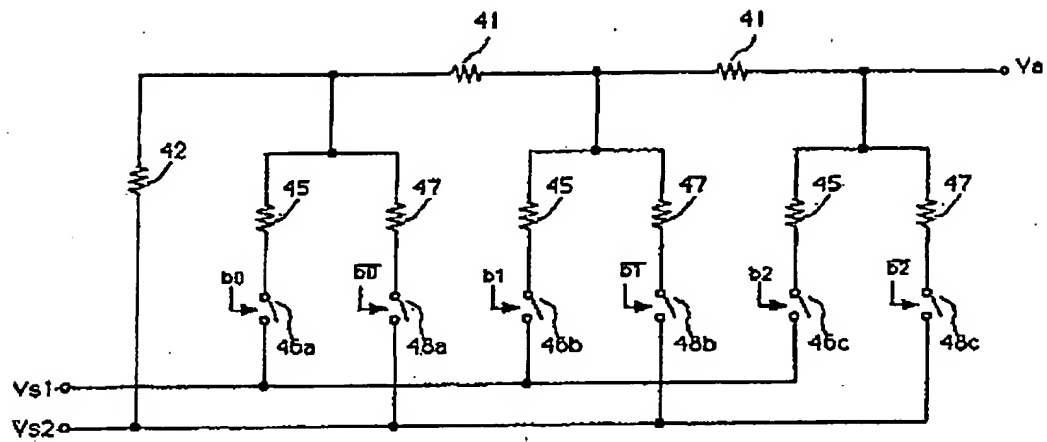
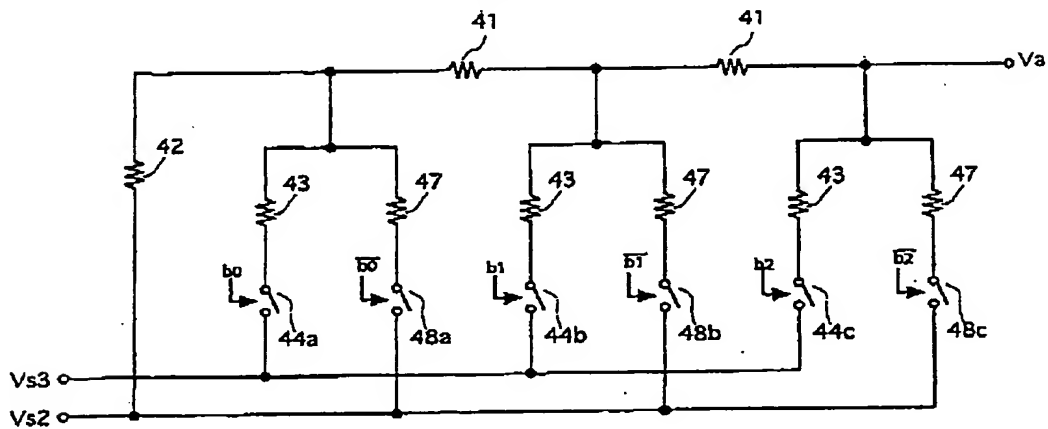


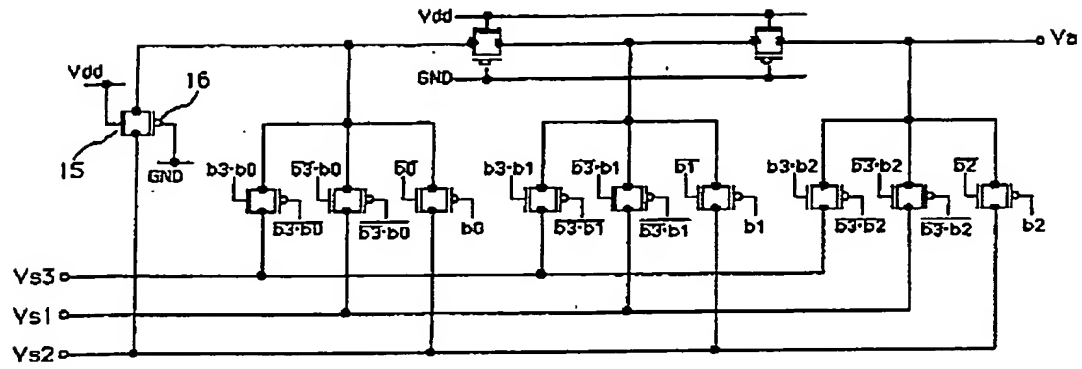
FIG. 23



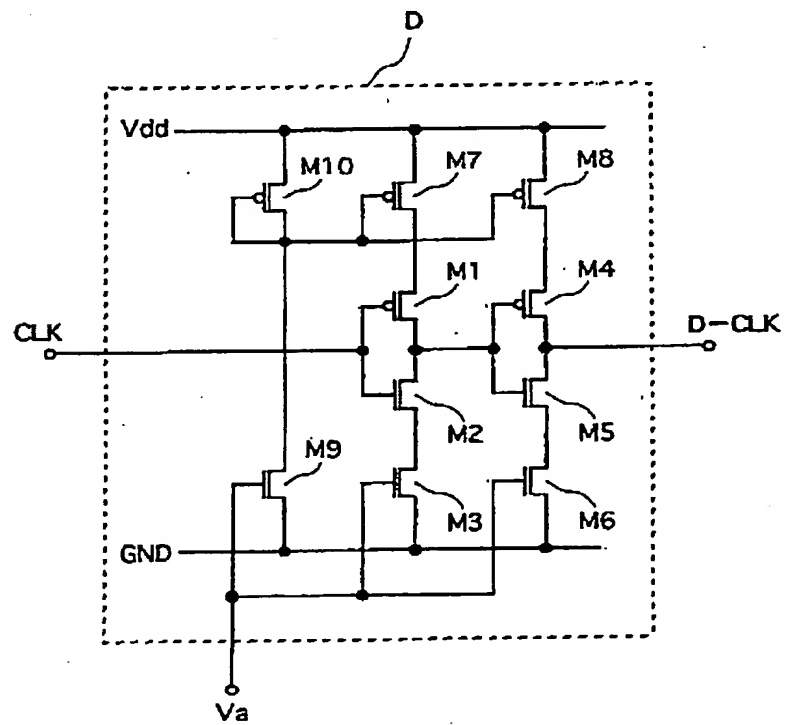




**FIG. 26**



**FIG. 27**



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FIG. 28

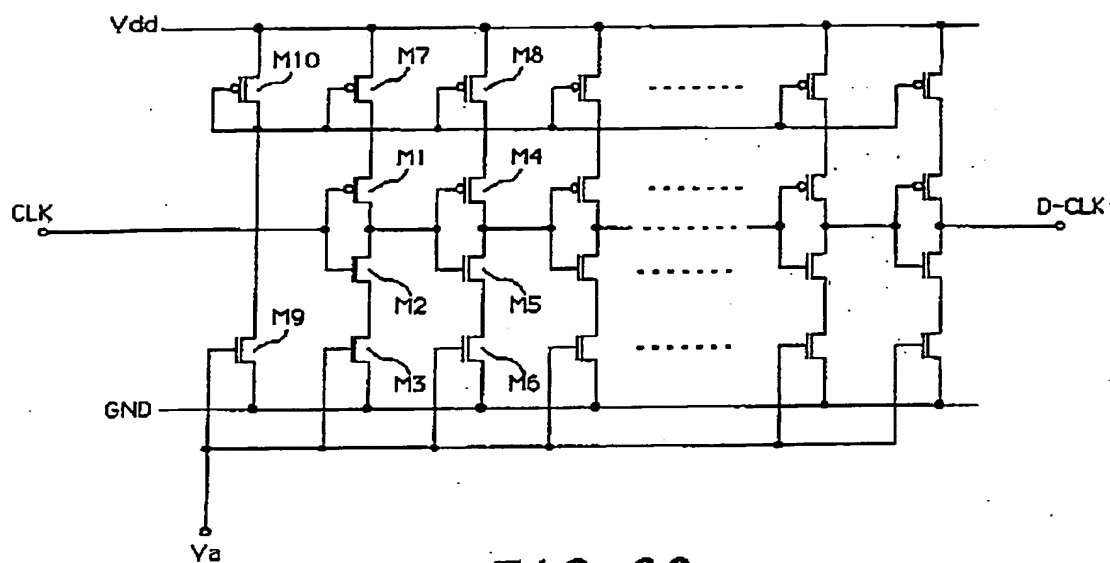
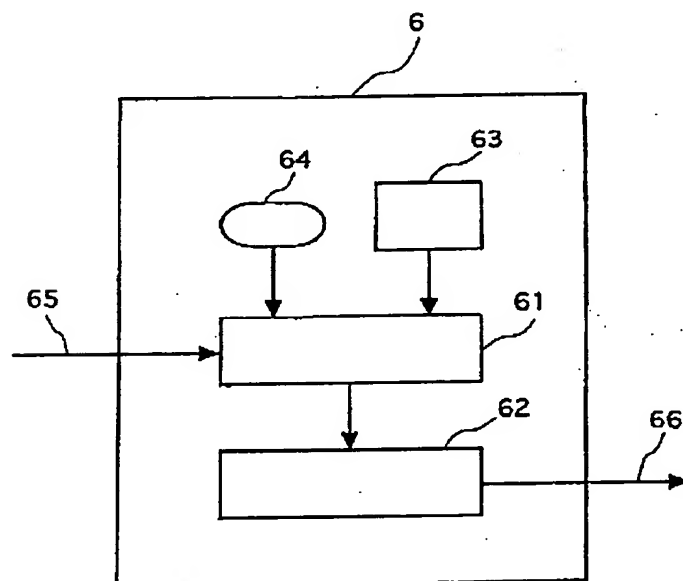


FIG. 29



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